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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,903	10/21/2005	Kazuto Hirokawa	2005-1624A	7960

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EXAMINER	
VINH, LAN	
ART UNIT	**PAPER NUMBER**
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,903	HIROKAWA ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34,36-38 and 40-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34, 36-38,40-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *102105*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 5-7, 9, 12-14, 17-18, 21-23, 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Farkas et al (US 6,573,173)

Farkas discloses a method for forming a copper interconnect using CMP, the interconnect recesses 50 being formed on a surface of an insulating material 47 and having a film of barrier material 85 formed on the surface of an insulating material. The method comprising:

polishing to eliminate a level difference in the surface of the interconnect material 63 to flatten the surface (fig. 6-7)

removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion of the copper/the copper becomes a thin film while applying a pressure of 4 psi/first pressure to the substrate (col 6, lines 41-62)

polishing to remove the interconnect material in the form of the thin film or remaining partly on the barrier material while applying a second pressure 0.5 psi, which is lower

than the first pressure, to the substrate, thereby exposing the barrier material 85 (col 7, lines 40-60)

simultaneously removing the unnecessary interconnect material and portions of the barrier material until the barrier material present in the non-interconnect region becomes a thin film while applying a pressure of 3 psi/ third pressure to the substrate (col 11, lines 50-60)

polishing, in a dielectric buffing step, to remove the unnecessary copper/interconnect material and the barrier material present in the non-interconnect region while applying a pressure of 0.4-0.5 psi/ fourth pressure, which is lower than the third pressure, to the substrate, thereby exposing the insulating material in the non-interconnect region (col 12, lines 12-25)

Regarding claim 2, fig.7 of Farkas shows that the unnecessary copper/interconnect material, the barrier material and the insulating material 47 are simultaneously removed by polishing

Regarding claims 5-6, 9, Farkas discloses carrying out a CMP to eliminate the level difference in the surface of the interconnect (col 5, lines 10-15)

Regarding claims 7,12-14, 17-18, 21-23, 26-28, Farkas discloses removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion by CMP utilizing a abasive-containing slurry (col 6, lines 30-35) which reads on carrying out the polishing by abrasive processing utilizing an electrostatic force/chemical etching

2. Claims 3-4, 42-44, 46, 49-51, 54-55, 58-60, 63-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Farkas et al (US 6,573,173)

Farkas discloses a method for forming a copper interconnect using CMP, the interconnect recesses 50 being formed on a surface of an insulating material 47 and having a film of barrier material 85 formed on the surface of an insulating material. The method comprising:

a first step of polishing to eliminate a level difference in the surface of the interconnect material 63 to flatten the surface (fig. 6-7)

a second step of removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion of the copper/the copper becomes a thin film while applying a pressure of 4 psi /first pressure to the substrate (col 6, lines 41-62)

a third step of polishing to remove the interconnect material in the form of the thin film or remaining partly on the barrier material while applying a second pressure 0.5 psi, which is lower than the first pressure, to the substrate, thereby exposing the barrier material 85 (col 7, lines 40-60)

a fourth step of simultaneously removing the unnecessary interconnect material and portions of the barrier material until the barrier material present in the non-interconnect region becomes a thin film while applying a pressure of 3 psi/ third pressure to the substrate (col 11, lines 50-60)

a fifth step of polishing, in a dielectric buffing step, to remove the unnecessary copper/interconnect material and the barrier material present in the non-interconnect

region while applying a pressure of 0.4-0.5 psi/ fourth pressure, which is lower than the third pressure, to the substrate, thereby exposing the insulating material in the non-interconnect region (col 12, lines 12-25)

Regarding claim 4, fig.7 of Farkas shows that the unnecessary copper/interconnect material, the barrier material and the insulating material 47 are simultaneously removed by polishing

Regarding claims 42-43, 46, 51, Farkas discloses carrying out a CMP to eliminate the level difference in the surface of the interconnect (col 5, lines 10-15)

Regarding claims 44 , 49, 50, 54, 58-59, 60, 63-65, Farkas discloses removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion by CMP utilizing a abasive-containing slurry (col 6, lines 30-35) which reads on carrying out the polishing by abrasive processing utilizing an electrostatic force/chemical etching

3. Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al (US 2003/0013387)

Tsai discloses a method for planarizing a surface using CMP, the surface includes the interconnect recesses 413 being formed on a surface of an insulating material 410 and having a film of barrier material 405 formed on the surface of an insulating material. The method comprising:

removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion of the

copper/the copper remains partly while applying a pressure of 0.8 psi/first pressure to the substrate (page 9, paragraph 0096-0097, 0100)

polishing to completely remove the interconnect material remaining partly on the barrier material while applying a second pressure 0.5 psi, which is lower than the first pressure, to the substrate, thereby exposing the underlying material in the non-interconnect region (page 9, paragraph 0101, fig. 3H)

4. Claims 29-34, 36-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Farkas et al (US 6,573,173)

Farkas discloses a method for forming a copper interconnect using CMP, the interconnect recesses 50 being formed on a surface of an insulating material 47 and having a film of barrier material 85 formed on the surface of an insulating material. The method comprising:

removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion of the copper/the copper becomes a thin film while applying a pressure of 4 psi/first pressure to the substrate (col 6, lines 41-62)

polishing to completely remove the interconnect material in the form of the thin film or remaining partly on the barrier material while applying a second pressure 0.5 psi, which is lower than the first pressure, to the substrate, thereby exposing the underlying material in the non-interconnect region (col 7, lines 40-60)

Regarding claim 30, Farkas discloses a step of polishing to eliminate a level difference in the surface of the interconnect material 63 to flatten the surface (fig. 6-7)

Regarding claims 31-32, Farkas discloses using optical endpoint detection to terminate the process when roughly 2000 angstroms/200 nm< 300 nm thickness of copper remains (col 6, lines 50-54, col 7, lines 1-3)

Regarding claim 33, Farkas discloses changing the chemical composition of the slurry resulting in more copper removal in step 17/ removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion of the copper step when compare to step 19/ polishing to completely remove the interconnect material in the form of the thin film step

Regarding claim 34, Farkas discloses removing the interconnect material until the copper/interconnect material present in the non-interconnect region of the substrate to remove a significant top portion by CMP utilizing a abasive-containing slurry /chemical liquid (col 6, lines 30-35)

Regarding claims 36-37, Farkas discloses removing the underlying material present in the non-interconnect region until a material 47 present under the underlying material becomes exposed (fig. 7)

5. Claim 38 is rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al (US 2003/0013387)

Tsai discloses a method for planarizing a surface using CMP, the surface includes the interconnect recesses 413 being formed on a surface of an insulating material 410

and having a film of barrier material 405 formed on the surface of an insulating material. The method comprising:

simultaneously removing the unnecessary interconnect material and barrier material until the barrier material present in the non-interconnect region of the substrate remains partly while applying a pressure of 0.8 psi/first pressure to the substrate (page 9, paragraph 0096-0097, 0100; fig. 3E)

removing the unnecessary interconnect material and the barrier material remaining partly while applying a pressure of 0.5 psi/second pressure, which is lower than the first pressure to the substrate, thereby exposing an underlying material present under the barrier material in the non-interconnect region (page 9, paragraph 0101; fig. 3G)

6. Claims 40-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Dubout et al (US 2003/0136684)

Dubout discloses a system for detecting endpoint for a CMP step, the system/apparatus comprises: an electrolytic processing section 132 confining electrolyte 120, provided with an end point detection device (fig. 3), for carrying out electrolytic processing of a substrate 113 held by a substrate holder 130 (page 5, paragraph 0055)

a CMP section 100, provided with an end point detection device (fig. 3), for carrying out chemical mechanical polishing of the substrate held by a substrate holder; and a carousel 111/substrate transfer device for transferring the substrate; wherein the

substrate is processed both in the electrolytic processing section and in the CMP section (page 3, paragraph 0034, 0036, 0039)

It is noted that according to the MPEP section 2114 [R-1] Apparatus and Article Claims — Functional Language

APPARATUS CLAIMS MUST BE STRUCTURALLY DISTINGUISHABLE FROM THE PRIOR ART

While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In regarding claim Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In regarding claim Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does"

MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. ex parte Marsham USPQ2d 1647 (Bd. Pat. App. & Inter. 1987)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 10-11, 15-16, 19-20, 24-25, 45, 47-48, 52-53, 56-57, 61-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farkas et al (US 6,573,173) in view of Yahalom et al (US 2003/0155255)

Farkas method has been described above. Unlike the instant claimed inventions as per claims 8,10-11, 15-16, 19-20, 24-25, 45, 47-48, 56-57, 61-62, Farkas fails to disclose removing the interconnect material by electrolytic processing utilizing a catalyst

Yahalom discloses a electropolishing method to polish a substrate having conductive layer, the method comprises a step of removing the conductive material by electrolytic processing utilizing a electropolishing solution (page 3, paragraphs 0033, 0035)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Farkas method by removing the interconnect material by electrolytic polishing/processing as per Yahalom since Yahalom teaches that eletropolishing method may be performed alone to planarize a substrate structure or may be performed in conjunction with subsequent CMP of the substrate structure to further reduce the step height and or remove excess material from the substrate (col 6, paragraph 0056)

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LV
April 23, 2007